In the Claims:

Please amend claims 1-4, 6, and 30-32. Please cancel claims 8-28 and 34-36 including both claims labeled "25. (Withdrawn)." Please add new claims 37-49.

The claims are as follows:

1. (Currently Amended) A method, comprising:

~~providing~~ forming an interlevel dielectric layer on a substrate;

forming a plurality of electrically conductive wires in said interlevel dielectric layer, top surfaces of said wires coplanar with a top surface of said interlevel dielectric layer;

forming a passivation layer on said top surfaces of said wires and said interlevel dielectric layer;

removing regions of said passivation layer to form via opening in said passivation layer over said plurality of wires, there being a respective via opening for each wire of said plurality of wires, said via openings extending from a top surface of said passivation layer to said top surfaces of said wires;

forming an electrically conductive layer on a top surface of said ~~substrate~~ passivation layer;

patterning said conductive layer into a plurality of wire bond pads spaced apart, each wire bond having first and second opposite ends, said top surface of said ~~substrate~~ passivation layer exposed between said wire bond pads, top surfaces of said wire bond pads being top surfaces of said patterned conductive layer and being parallel to said top surface of said substrate, said first ends of each wire bond pad of said plurality of wire bond pads extending over a respective via opening, filling said via opening and electrically contacting a respective wire of said plurality of wires;

after said patterning, forming a first dielectric layer directly on said top surface of said ~~substrate~~ passivation layer in spaces between said wire bond pads, on all sidewalls of said wire bond pads, and directly on said top surfaces of said wire bond pads, said first dielectric layer not filling said spaces between adjacent sides of said wire bond pads; ~~and~~

after said forming said first dielectric layer, forming a second dielectric layer on a top surface of said first dielectric layer, said second dielectric layer filling remaining spaces between adjacent sidewalls of said wire bond pads; and

after said forming said second dielectric layer, completely removing said first and second dielectric layers from said top surfaces of ~~said conductive layer of~~ said wire bond pads, ~~top surfaces of said dielectric layer in said spaces~~ newly formed top surfaces of said first and second dielectric layers coplanar with said top surfaces of said wire bond pads.

2. (Currently Amended) The method of claim 1, further including:

after said completely removing said first and second dielectric layers from said top surfaces of said wire bond pads, recessing said first and second dielectric layers ~~in said spaces~~ below said top surfaces of said wire bond pads, an upper region of sidewalls of said wire bond pads exposed in said spaces and a lower region of said sidewalls of said wire bond pads covered by said first dielectric layer.

3. (Currently Amended) The method of claim 1, further including:

after said completely removing said first and second dielectric layers from said top surfaces of said wire bond pads, recessing said wire bond pads below said newly formed top surfaces of said first and second dielectric layers ~~in said spaces after said completely removing said dielectric layer from said top surfaces of said wire bond pads~~.

4. (Currently Amended) The method of claim 1, further including:

after said completely removing said first and second dielectric layers from said top surfaces of said wire bond pads, forming a final dielectric layer on ~~said substrate,~~ said first and second dielectric layers and said wire bond pads; and

forming pad openings in said final dielectric layer to expose less than an entire portion of each said wire bond pad of said plurality of wire bond pads in said pad openings and to expose regions of said first and second dielectric layers between wire bond pads, said final dielectric layer extending over said first and second ends of said wire bond pads and over said via openings.

5. (Original) The method of claim 4, wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide.

6. (Currently Amended) The method of claim 1, wherein said first dielectric layer comprises a layer of silicon oxide[[,]] and said second dielectric layer comprises a layer of silicon nitride ~~or combinations thereof~~.

7. (Original) The method of claim 1, wherein said wire bond pads comprise aluminum, aluminum copper alloy, copper, gold, tantalum, tantalum nitride or combinations thereof.

8-29 (Canceled)

30. (Currently Amended) The method of claim 1, wherein said ~~dielectric layer comprises a first dielectric layer over a conformal dielectric layer, a~~ said newly formed top surface of said first dielectric layer completely surrounds ~~surrounding a~~ said newly formed top surface of said second dielectric layer~~, said top surfaces of said first and second dielectric layers being coplanar and parallel to said top surface of said substrate~~.

31. (Currently Amended) The method of claim 30, wherein said ~~top surfaces of both said first and second dielectric layers are coplanar with said top surfaces of said wire bond pads~~ forming a plurality of electrically conductive wires includes:

forming trenches in said interlevel dielectric layer;

filling said trenches with an electrically conductive material; and

performing a chemical-mechanical polishing.

32. (Currently Amended) The method of claim 1, wherein said completely removing said first and second dielectric layers from said top surfaces of said wire bond pads includes:

performing a chemical-mechanical polishing.

33-36 (Canceled)

37. (New) The method of claim 4, wherein said final dielectric layer extends over said via openings.

38. (New) The method of claim 1, further including:

after said completely removing said first and second dielectric layers from said top surfaces of said wire bond pads, forming a final dielectric layer on said first and second dielectric layers and said wire bond pads;

forming pad openings in said final dielectric layer to expose less than an entire portion of each wire bond pad of said plurality of wire bond pads in said pad openings and to expose regions of said first and second dielectric layers between said wire bond pads, said final dielectric layer extending over said first and second ends of wire bond pads and over said via openings; and

after forming said pad openings, recessing portions of said wire bond pads not covered by said final dielectric below said newly formed top surfaces of said first and second dielectric layers.

39. (New) The method of claim 38, wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide

40. (New) The method of claim 1, further including:

after said completely removing said first and second dielectric layers from said top surfaces of said wire bond pads, recessing said wire bond pads below said newly formed top surfaces of said first and second dielectric layers.

after said recessing said wire bond pads, forming a final dielectric layer on said first and second dielectric layers and said wire bond pads; and

after forming said final dielectric layer, forming pad openings in said final dielectric layer to expose less than an entire portion of each said wire bond pad of said plurality of wire bond pads in said pad openings and to expose regions of said first and second dielectric layers between

said wire bond pads, said final dielectric layer extending over said first and second ends of wire bond pads and over said via openings.

41. (New) The method of claim 40, wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide

42. (New) A method, comprising:

forming an interlevel dielectric layer on a substrate;

forming a plurality of electrically conductive wires in said interlevel dielectric layer, top surfaces of said wires coplanar with a top surface of said interlevel dielectric layer;

forming a passivation layer on said top surfaces of said wires and said interlevel dielectric layer;

removing regions of said passivation layer to form via opening in said passivation layer over said plurality of wires, there being a respective via opening for each wire of said plurality of wires, said via openings extending from a top surface of said passivation layer to said top surfaces of said wires;

forming an electrically conductive layer on a top surface of said passivation layer;

patterning said conductive layer into a plurality of wire bond pads spaced apart, each wire bond having first and second opposite ends, said top surface of said passivation layer exposed between said wire bond pads, top surfaces of said wire bond pads being top surfaces of said conductive layer and being parallel to said top surface of said substrate, said first ends of each wire bond pad of said plurality of wire bond pads extending over a respective via opening, filling said via opening and electrically contacting a respective wire of said plurality of wires;

after said patterning, forming a first dielectric layer directly on said top surface of said passivation layer in spaces between said wire bond pads, on all sidewalls of said wire bond pads, and directly on said top surfaces of said wire bond pads, said first dielectric layer not filling said spaces between adjacent sides of said wire bond pads;

after said forming said first dielectric layer, forming a second dielectric layer on a top surface of said first dielectric layer, said second dielectric layer filling remaining spaces between adjacent sidewalls of said wire bond pads;

forming a final dielectric layer on said first and second dielectric layers and said wire bond pads;

forming pad openings in said final dielectric layer to expose less than an entire portion of each said wire bond pad of said plurality of wire bond pads in said pad openings and to expose regions of said first and second dielectric layers between wire bond pads, said final dielectric layer extending over said first and second ends of said wire bond pads and over said via openings; and

after said forming said pad openings in said final dielectric layer, removing said first and second dielectric layers from said top surfaces of said wire bond pads where said first and second dielectric layers are not covered by said final dielectric layer, newly formed top surfaces of said first and second dielectric layers coplanar with said top surfaces of said wire bond pads where said first and second dielectric layers are not covered by said final dielectric layer, regions of said first and second dielectric layers extending over said first and second ends of said wire bond pads and said via openings.

43. (New) The method of claim 42, further including:

after said removing said first and second dielectric layers from said top surfaces of said wire bond pads, recessing said first and second dielectric layers below said top surfaces of said wire bond pads in regions of said first and second dielectric layer not covered by said final dielectric layer, an upper region of sidewalls of said bond pads exposed in said spaces and a lower region of said sidewalls of said bond pads covered by said first dielectric layer.

44. (New) The method of claim 42, further including:

after said removing said first and second dielectric layers from said top surfaces of said wire bond pads, recessing said wire bond pads below said newly formed top surfaces of said first and second dielectric layers, in regions of said wire bond pads not covered by said first and second dielectric layers.

45. (New) The method of claim 42, wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide.

46. (New) The method of claim 42, wherein said first dielectric layer comprises a layer of silicon oxide and said second dielectric layer comprises a layer of silicon nitride.

47. (New) The method of claim 42, wherein said wire bond pads comprise aluminum, aluminum copper alloy, copper, gold, tantalum, tantalum nitride or combinations thereof.

48. (New) The method of claim 42, wherein said newly formed top surface of said first dielectric layer completely surrounds said newly formed top surface of said second dielectric layer.

49. (New) The method of claim 42, wherein said forming a plurality of electrically conductive wires includes:

forming trenches in said interlevel dielectric layer;

filling said trenches with an electrically conductive material; and

performing a chemical-mechanical polishing.